AN11547

BGA3021 - 1.2 GHz 16 dB gain CATV amplifier

Rev. 1 — 16 September 2014

Application note

Document information

Info	Content
Keywords	BGA3021, Evaluation board, CATV, Medium Power
Abstract	This application note describes the schematic and layout requirements for using the BGA3021 as a CATV medium power amplifier.

Revision history

Rev	Date	Description
1	20140916	First publication

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1. Introduction

The BGA3021 customer evaluation board enables the user to evaluate the performance of the medium power wideband CATV MMIC amplifier BGA3021.

The BGA3021 performance information is available in the BGA3021 datasheet.

This application note describes the evaluation board schematic and layout requirements for using the BGA3021 as a CATV medium power amplifier between 40 MHz and 1200 MHz. The BGA3021 is fabricated in the BiCMOS process and packaged in a lead-free 8-pin SOT786-2 package. The BGA3021 is surface-mounted on an evaluation board with element matching and DC decoupling circuitry. The amplifier MMIC comprises a push-pull amplifier with internal bias network and operates over a frequency range of 40 MHz to 1200 MHz with a supply voltage between 5 V and 8 V.

2. System features

- 16 dB gain
- Internally biased and internal integrated feedback
- Frequency range of 40 MHz to 1200 MHz
- High linearity with an $IP3_o$ of 47 dBm and $IP2_o$ of 85 dBm
- Operating from 5 V to 8 V supply
- High gain output 1 dB compression point of 30 dBm
- 75 Ω input and output impedance
- Unconditionally stable
- Icc(tot) can be controlled between 175 mA and 350 mA

3. Customer evaluation kit contents

The evaluation kit contains the following items:

- ESD safe casing
- BGA3021 evaluation board

4. Application Information

For evaluation purposes an evaluation board is available. The evaluation circuit can be seen in figure 1 and the corresponding PCB is shown in figure 2. Table 1 shows the bill of materials.

4.1 Evaluation board circuit

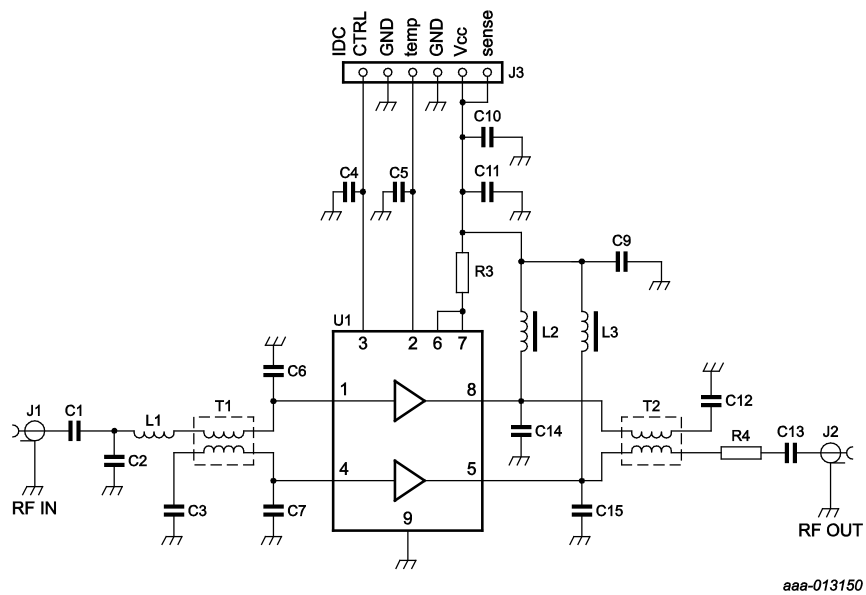


Fig 1. BGA3021 evaluation circuit

The power supply is applied on the Vcc pin of connector J3 and is applied to the BGA3021 via chokes L2 and L3 which provides RF blocking to the supply line. Capacitors C9, C10 and C11 are supply decoupling capacitors, where C4 and C5 are decoupling capacitors for the control lines.

At the F-connector J1 the RF input signal is applied where capacitor C1 provides DC-blocking, followed by C2 and L1 for input matching (Z = 75 Ω). The single ended unbalanced 75 Ω signal is converted into a balanced signal for push pull configuration. The balanced signal is applied to the input of BGA3021 at pin 1 and pin 4. Capacitor C3 provides DC-blocking. Capacitors C6 and C7 add extra capacitance to the output of balun T1, which results in improved input matching.

At the output the amplified balanced signal are converted back into one 75 Ω single ended signal by balun T2. Capacitors C14 and C15 add extra capacitance to the balun for improved impedance matching. Capacitors C12 and C13 are DC-blocking capacitors. Resistor R4 is a 0 Ω jumper and has no function other than passing the RF signal.

Resistor R3 provides a protection against damaging the internal crowbar due to overshoot of the supply during switch on or switch off. This resistors needs to be in the circuit to guarantee resistance against electrical overstress.

The Icc can be controlled via the IDC CTRL pin of connector J3. The high current mode (350 mA) can be selected by leaving the IDC CTRL pin open or by applying 3.3V.The low current mode can be selected by applying 0 V to the IDC CTRL pin.

The Temp pin on connector J3 gives access to an internal temperature sense diode which can be used to verify proper thermal connection of the exposed die pad. The use of this function is described in chapter 4.3

4.2 Choice of balun

The choice of balun is important when the maximum performance needs to be achieved, especially on input and output return loss. Investigation showed that to get the best output performance, balun type MABA-010245 should be used. This balun gives a good output return loss and because of its low losses also give maximum P1dB, IP2 and IP3 levels.

However, balun type MABA-010245 does not give the best input return loss. Balun type MABA-007159 with slightly more losses gives a much better input return loss. The extra losses do not have any impact on the distortion values as it is placed at the input of the device. The noise figure will slightly increase but is not a problem as the BGA3021 will be used as final amplifier. For a system solution with low noise and more total gain the BGA3018 can be used in front of the BGA3021.

Baluns also play a big role in the frequency coverage range. For frequencies lower than 40 MHz the BGA3021 can be made to work with the use of MABA-007532. Lab samples show functionality between 5 MHz and 200 MHz with the use of MABA-007532 at the input and output.

4.3 Temperature sense

Pin 2 of the BGA3021 gives access to a thermal diode which can be used to measure the temperature increase between power-off state and power-on state. This can be very helpful to check if the exposed die-pad has a good solder connection to the circuit board. In case the solder connection has thermal voids a rapid increase in temperature can be noticed.

A proposed circuit can be seen in fig 2.
During the whole test procedure a 1 mA current should be applied at pin 2. The Voltage level Vtemp will represent the actual die temperature.

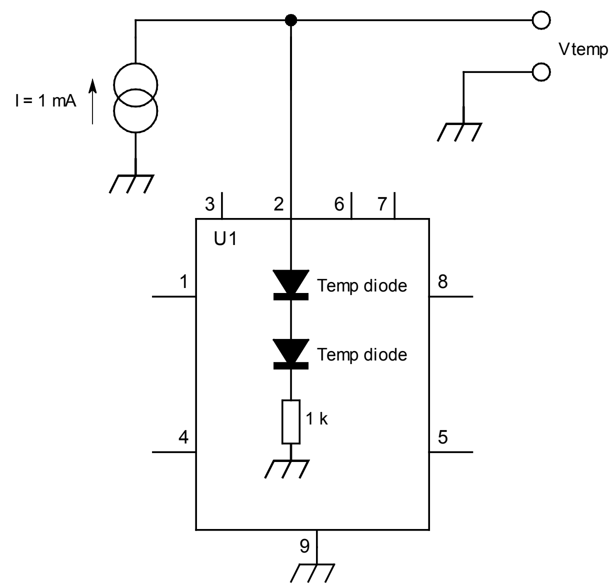


Fig 2. Temperature sense circuit

To check for any thermal solder voids the following procedure need to be followed:

Step 1: At power-off state and in room temperature measure Vtemp
Step 2: Power on the device
Step 3: Wait 1 second to let the device heat up.
Step 4: Measure Vtemp again
Step 5: Switch off power

The Vtemp Voltage difference between power-off and power-on will be about 200mV for a device without thermal voids. When the Voltage difference is higher the thermal connection is not good and performance cannot be guaranteed.

4.4 Evaluation board layout

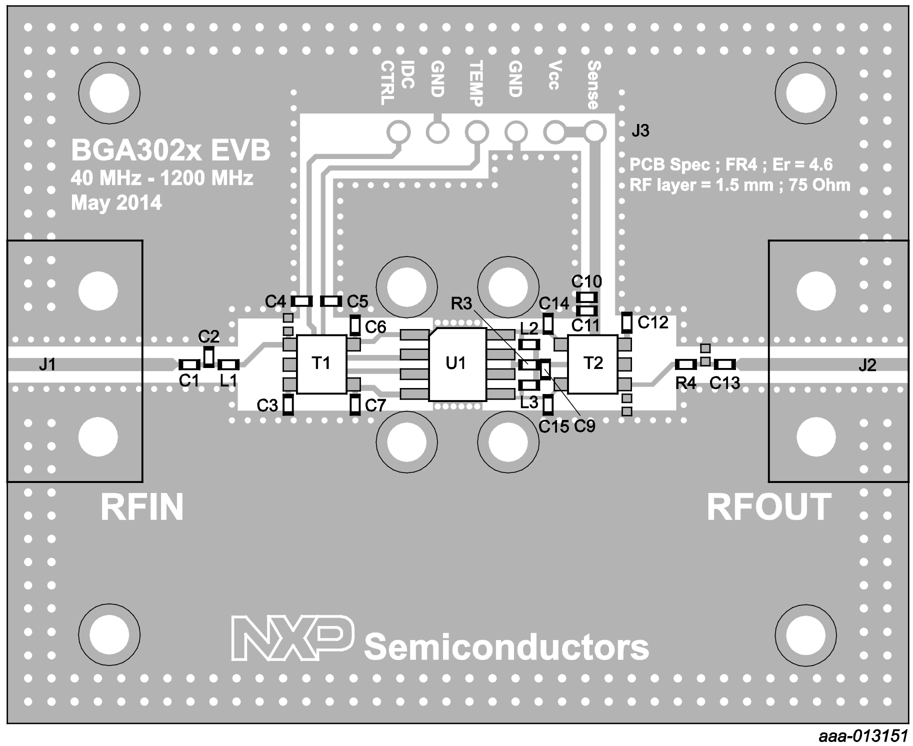


Fig 3. BGA3021 evaluation board layout

For optimum distortion performance it is important to have enough ground vias underneath and around the MMICs ground pins. This lowers the inductance to the ground plane. The evaluation board is made with two layer FR4 material.

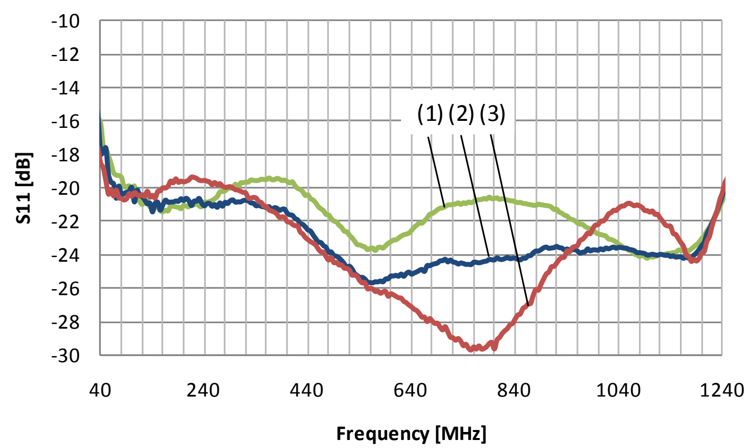
4.5 Bill of materials

Table 1. Evaluation board BOM

Circuit Reference	Description	Qty	Mfr	Manufacturer number	Supplier	Supplier part number
C1, C3, C4, C5, C9, C11, C12, C13	10 nF	8	Murata	GRM155R71E103KA01D	Digikey	490-1312-1-ND
C2	0.47 pF	1	Phycomp	2238 869 14477	Phycomp	2238 869 14477
C8, C10	100 nF	2	Murata	GRM155R61A104KA01D	Digikey	490-1318-2-ND
C6, C7, C14, C15	1 pF	4	Murata	GRM1555C1H1R0CA01D	Digikey	490-3199-1-ND
L1	1.0 nH	1	Murata	LQG15HS1N0S02D	Digikey	490-2610-1-ND
L2, L3	Choke	2	Murata	BLM15HD182SN1D	Digikey	490-5196-1-ND
R1	3300 Ω	1	Yageo	RC0402FR-073K3L	Digikey	311-3.30KLRTR-ND
R2	4700 Ω	1	Yageo	RC0402FR-074K7L	Digikey	311-4.7KLRTR-ND
R3	15 Ω	1	Yageo	RC0402FR-0715RL	Digikey	311-15LRCT-ND
R4	0 Ω Jumper	1	Murata	RC0402JR-070RL	Digikey	311-0.0JRTR-ND
J1, J2	75 Ω F-connector	2	Bomar	861V509ER6	Mouser	678-861V509ER6
J3	Header 6-pin	1	Molex		Digikey	WM2748-ND
T1	Balun transformer	1	MACOM	MABA-007159-000000	Mouser	937-MABA007159000000
T2	Balun transformer	1	MACOM	MABA-010245-CT1160	Mouser	937-MABA010245CT1160
U1	BGA3021	1	NXP	BGA3021	NXP	BGA3021

5. Measurement results

5.1 S-Parameters

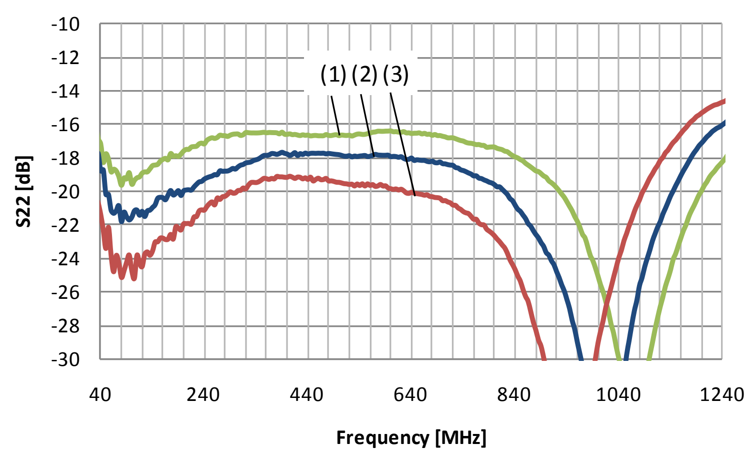


(1) Tamb = -40 °C

(2) Tamb = +25 °C

(3) Tamb = +85 °C

Fig 4. Input matching (S11); Vcc = 8 V, IDC CTRL = 3.3 V or open

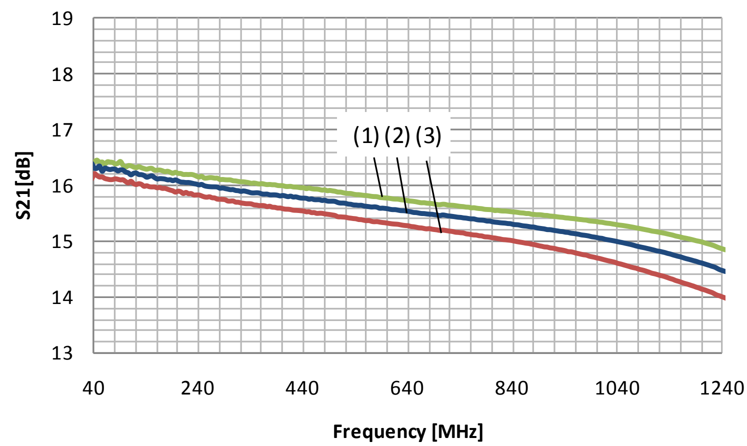


(1) Tamb = -40 °C

(2) Tamb = +25 °C

(3) Tamb = +85 °C

Fig 5. Output matching (S22); Vcc = 8 V, IDC CTRL = 3.3 V or open

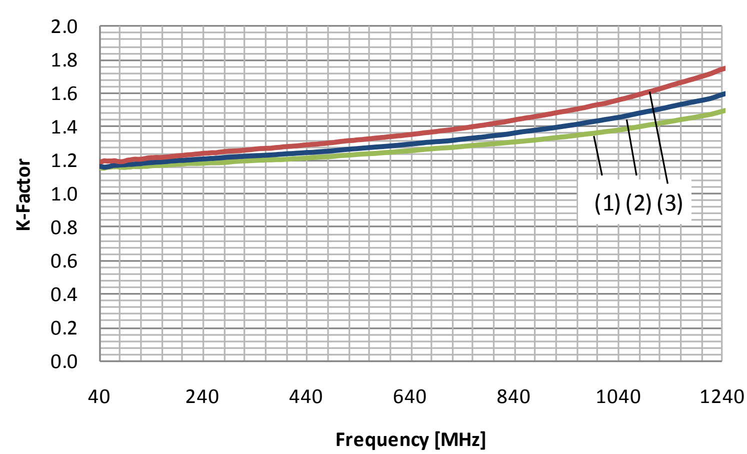


(1) Tamb = -40 °C

(2) Tamb = +25 °C

(3) Tamb = +85 °C

Fig 6. Gain (S21); Vcc = 8 V, IDC CTRL = 3.3 V or open

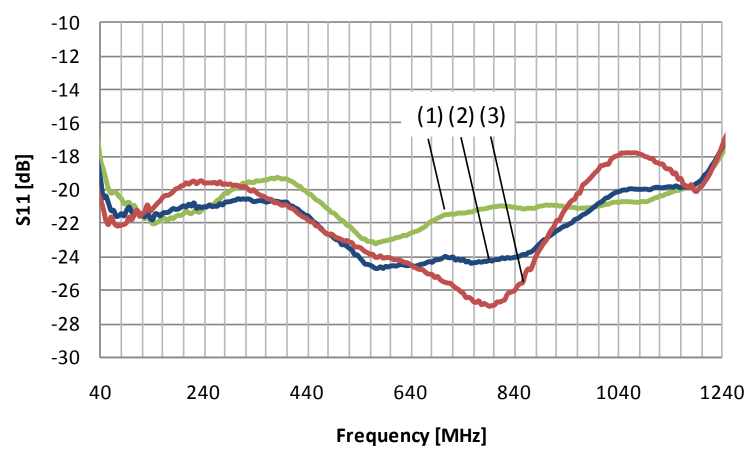


(1) Tamb = -40 °C

(2) Tamb = +25 °C

(3) Tamb = +85 °C

Fig 7. K-factor; Vcc = 8 V, IDC CTRL = 3.3 V or open

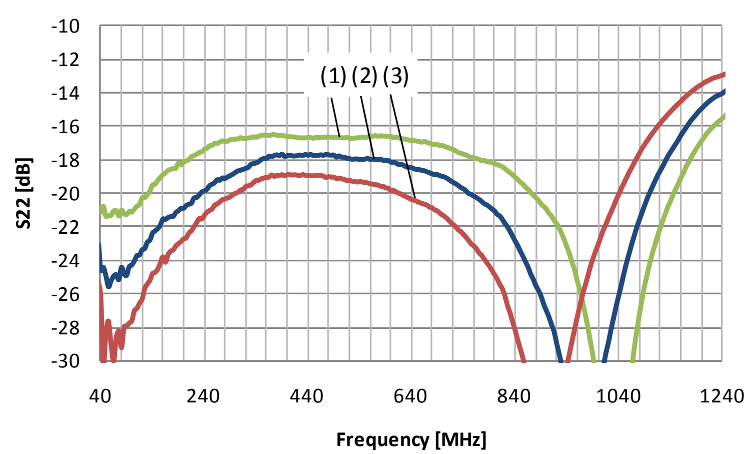


(1) Tamb = -40 °C

(2) Tamb = +25 °C

(3) Tamb = +85 °C

Fig 8. Input matching (S11); Vcc = 8 V, IDC CTRL = 0 V

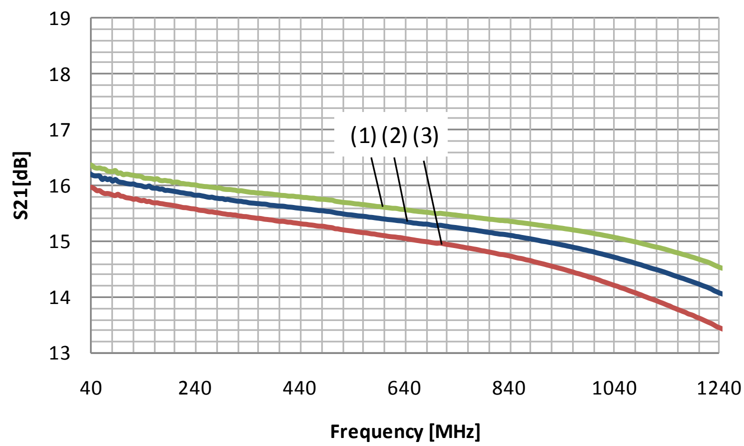


(1) Tamb = -40 °C

(2) Tamb = +25 °C

(3) Tamb = +85 °C

Fig 9. Output matching (S22); Vcc = 8 V, IDC CTRL = 0 V

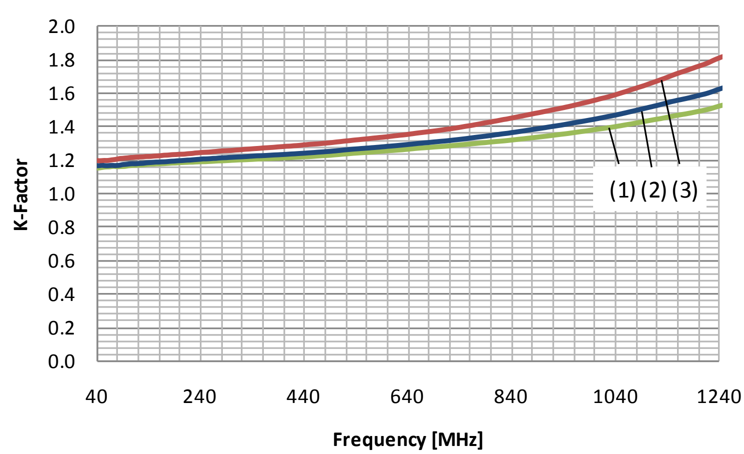


(1) Tamb = -40 °C

(2) Tamb = +25 °C

(3) Tamb = +85 °C

Fig 10. Gain (S21); Vcc = 8 V, IDC CTRL = 0 V

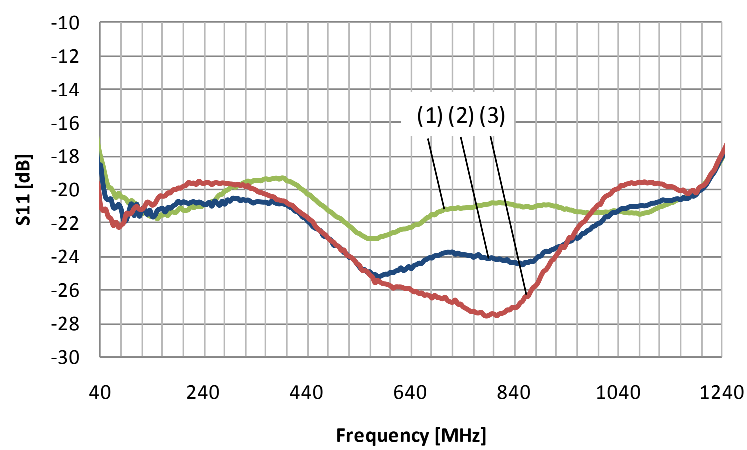


(1) Tamb = -40 °C

(2) Tamb = +25 °C

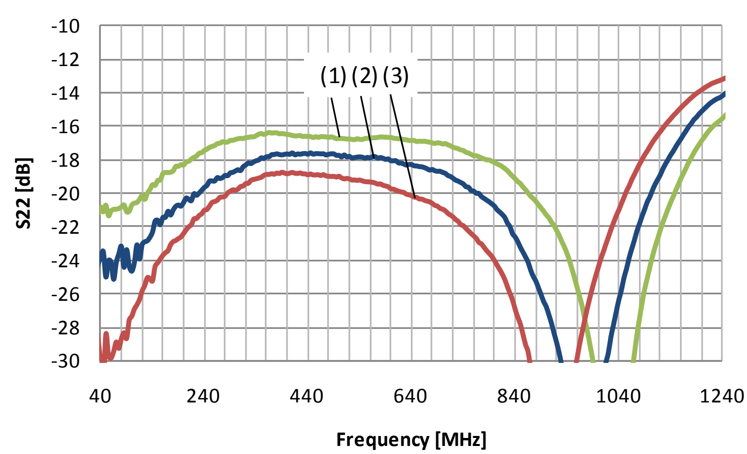
(3) Tamb = +85 °C

Fig 11. K-factor; Vcc = 8 V, IDC CTRL = 0 V



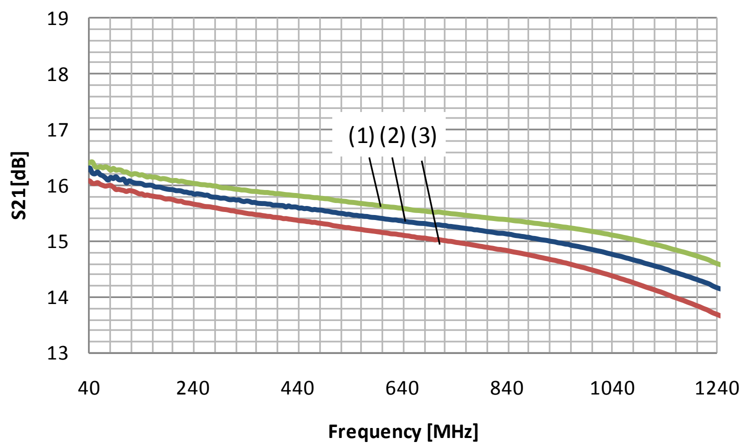
(1) Tamb = -40 °C
(2) Tamb = +25 °C
(3) Tamb = +85 °C

Fig 12. Input matching (S11); Vcc = 5 V, IDC CTRL = 0 V



(1) Tamb = -40 °C
(2) Tamb = +25 °C
(3) Tamb = +85 °C

Fig 13. Output matching (S22); Vcc = 5 V, IDC CTRL = 0 V

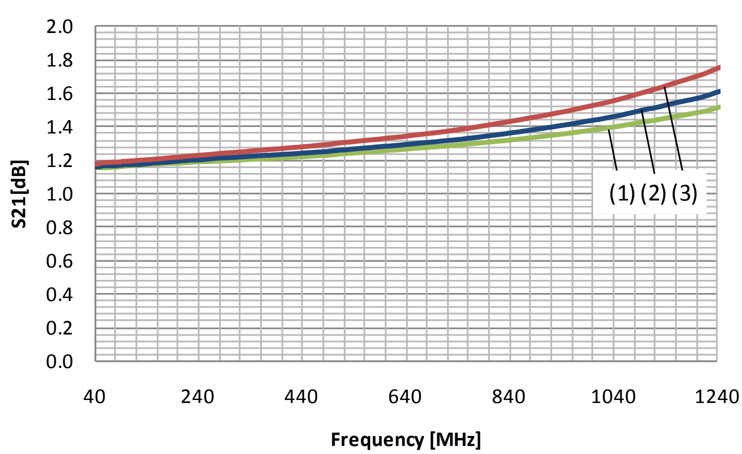


(1) Tamb = -40 °C

(2) Tamb = +25 °C

(3) Tamb = +85 °C

Fig 14. Gain (S21); Vcc = 5 V, IDC CTRL = 0 V



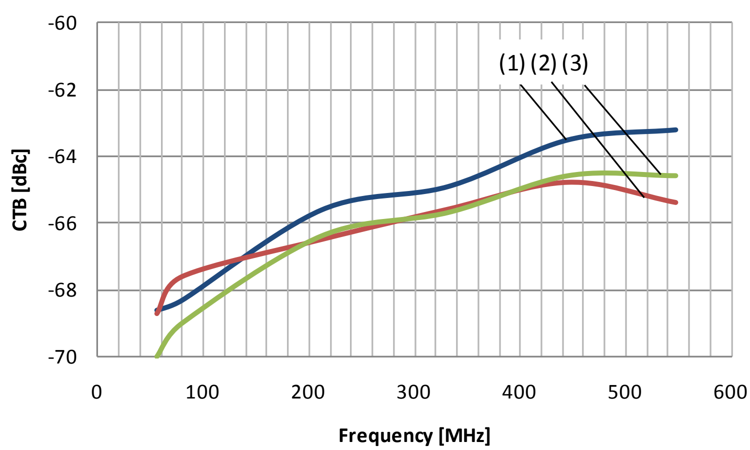
(1) Tamb = -40 °C

(2) Tamb = +25 °C

(3) Tamb = +85 °C

Fig 15. K-factor; Vcc = 5 V, IDC CTRL = 0 V

5.2 Distortion



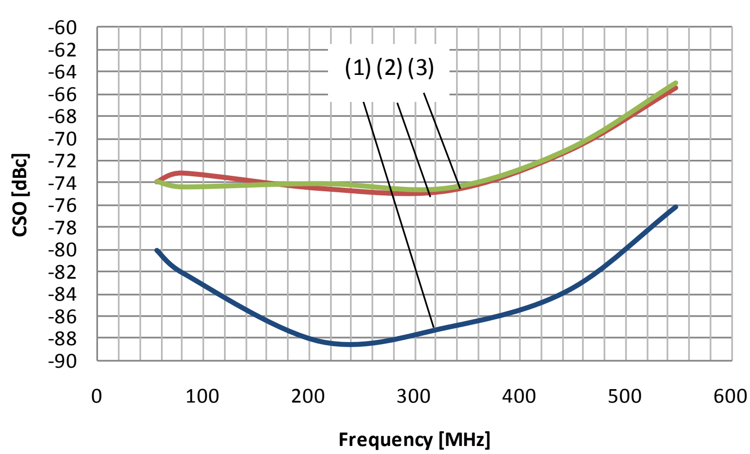
(1) Vcc = 8 V, IDC CTRL = 3.3V or open

(2) Vcc = 8 V, IDC CTRL = 0 V (Low current mode)

(3) Vcc = 5 V, IDC CTRL = 0 V (Low current mode)

79 channels NTSC , Vo = 43 dBmV, Tamb = +25 °C

Fig 16. Composite triple beat (CTB)



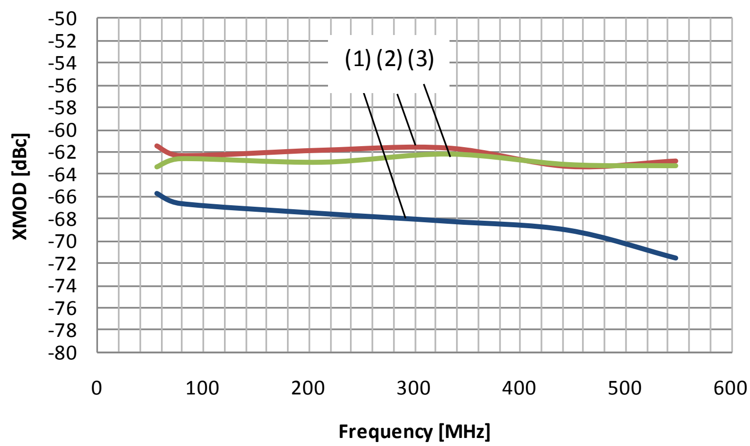
(1) Vcc = 8 V, IDC CTRL = 3.3V or open

(2) Vcc = 8 V, IDC CTRL = 0 V

(3) Vcc = 5 V, IDC CTRL = 0 V

79 channels NTSC , Vo = 43 dBmV, Tamb = +25 °C

Fig 17. Composite second order (CSO)



(1) Vcc = 8 V, IDC CTRL = 3.3V or open

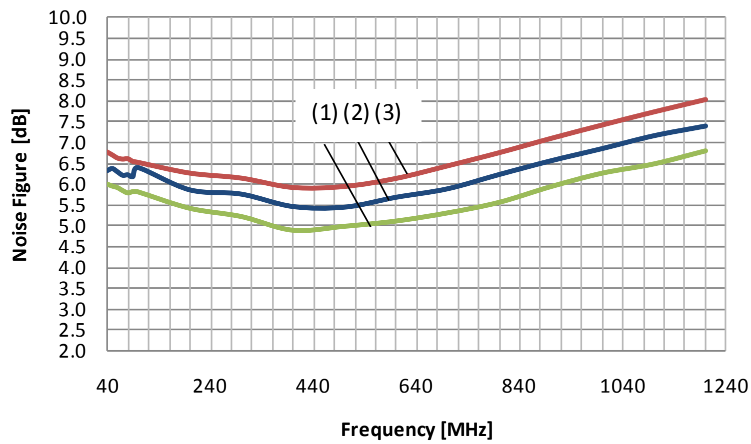
(2) Vcc = 8 V, IDC CTRL = 0 V

(3) Vcc = 5 V, IDC CTRL = 0 V

79 channels NTSC , Vo = 43 dBmV, Tamb = +25 °C

Fig 18. Cross modulation (XMOD)

5.3 Noise figure

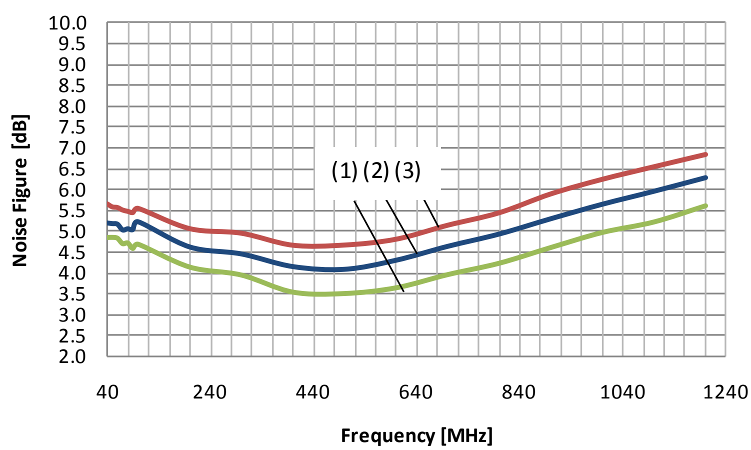


(1) Tamb = -40 °C

(2) Tamb = +25 °C

(3) Tamb = +85 °C

Fig 19. Noise figure (NF); Vcc = 8 V, IDC CTRL = 3.3V or open

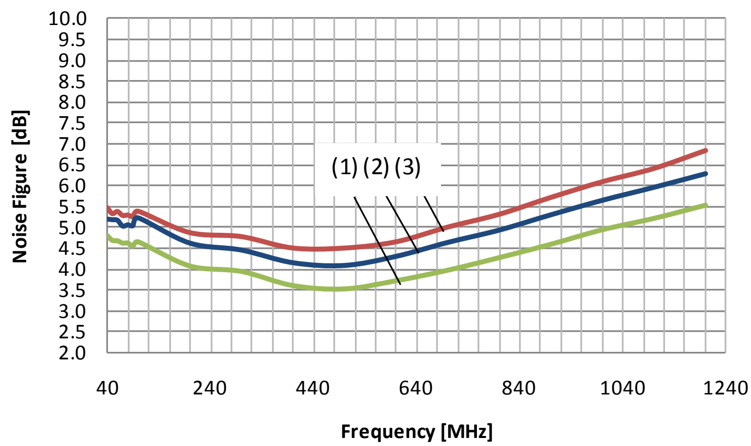


(1) Tamb = -40 °C

(2) Tamb = +25 °C

(3) Tamb = +85 °C

Fig 20. Noise figure (NF); Vcc = 8 V, IDC CTRL = 0V



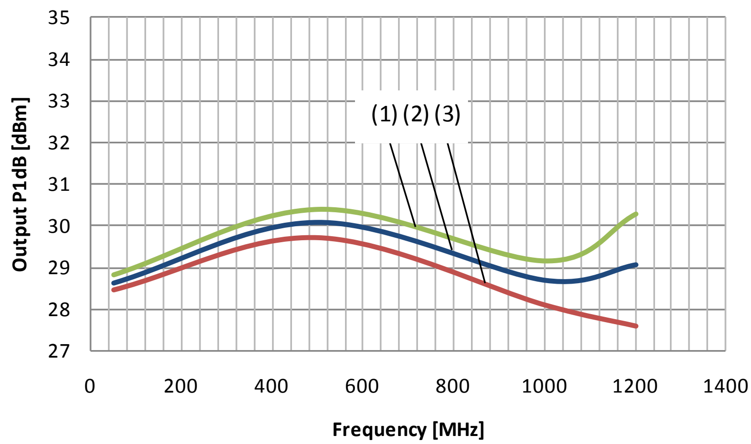
(1) Tamb = -40 °C

(2) Tamb = +25 °C

(3) Tamb = +85 °C

Fig 21. Noise figure (NF); Vcc = 5 V, IDC CTRL = 0V

5.4 Output P1dB

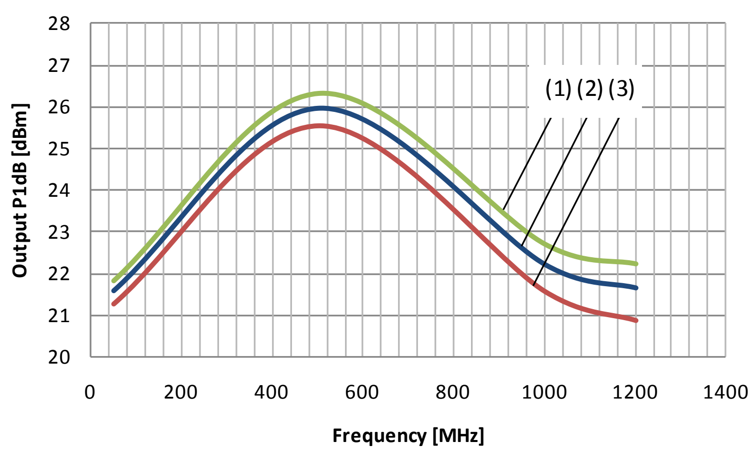


(1) Tamb = -40 °C

(2) Tamb = +25 °C

(3) Tamb = +85 °C

Fig 22. Output P1dB; Vcc = 8 V, IDC CTRL = 3.3 V or open

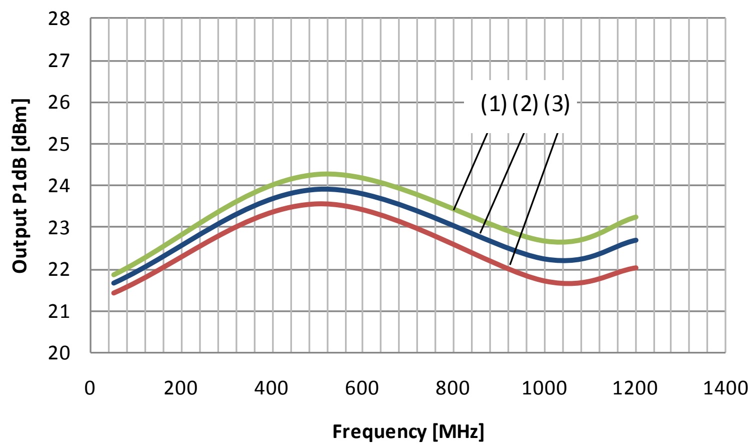


(1) Tamb = -40 °C

(2) Tamb = +25 °C

(3) Tamb = +85 °C

Fig 23. Output P1dB; Vcc = 8 V, IDC CTRL = 0 V



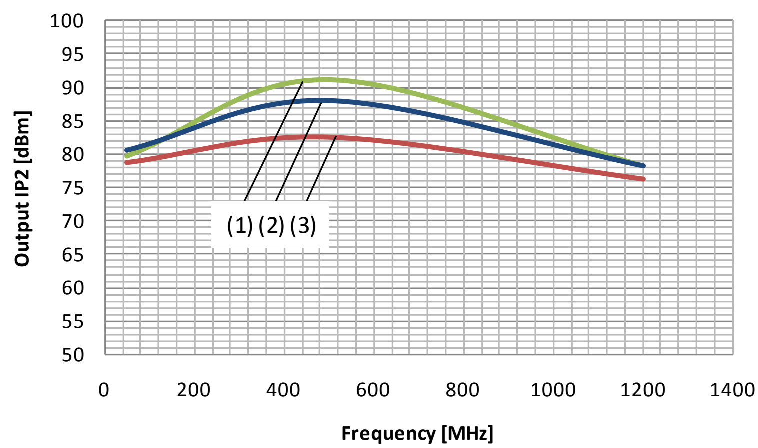
(1) Tamb = -40 °C

(2) Tamb = +25 °C

(3) Tamb = +85 °C

Fig 24. Output P1dB; Vcc = 5 V, IDC CTRL = 0 V

5.5 Output IP2



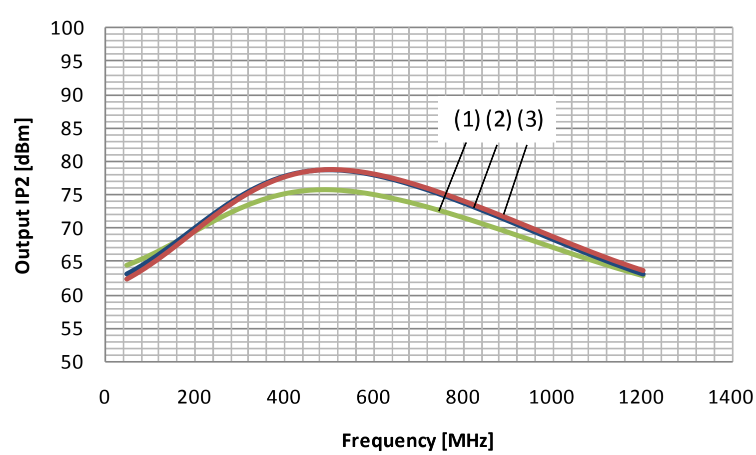
a. Output power = 10 dBm per frequency.

(1) Tamb = -40 °C

(2) Tamb = +25 °C

(3) Tamb = +85 °C

Fig 25. Output IP3; Vcc = 8 V, IDC CTRL = 3.3 V or open



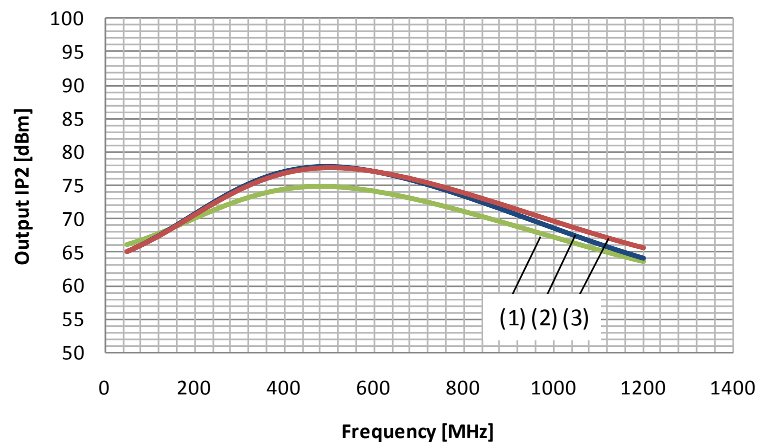
a. Output power = 10 dBm per frequency.

(1) Tamb = -40 °C

(2) Tamb = +25 °C

(3) Tamb = +85 °C

Fig 26. Output IP2; Vcc = 8 V, IDC CTRL = 0



a. Output power = 10 dBm per frequency.

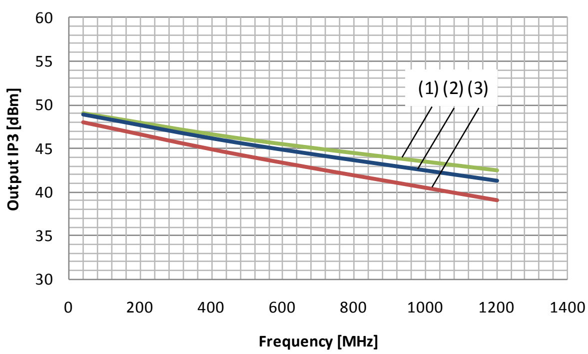
(1) Tamb = -40 °C

(2) Tamb = +25 °C

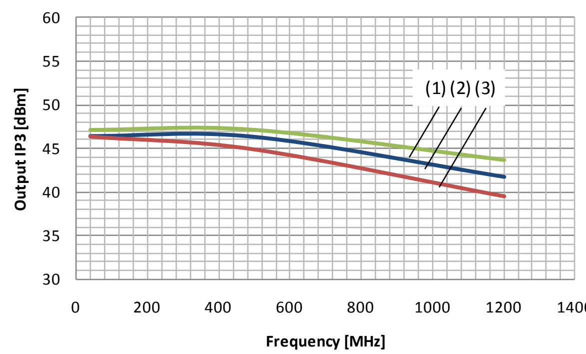
(3) Tamb = +85 °C

Fig 27. Output IP2; Vcc = 5 V, IDC CTRL = 0 V

5.6 Output IP3



a. f2 = f1 ± 1 MHz , output power = 10 dBm per frequency.



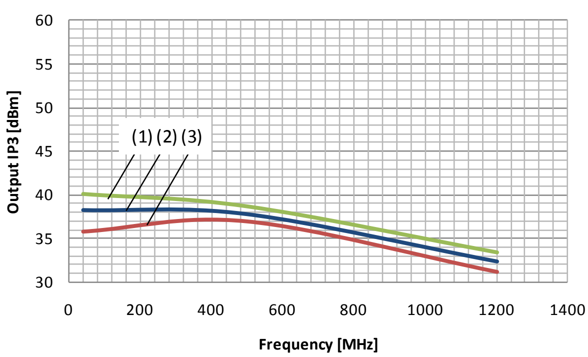
b. f2 = f1 ± 6 MHz , output power = 10 dBm per frequency.

(1) Tamb = -40 °C

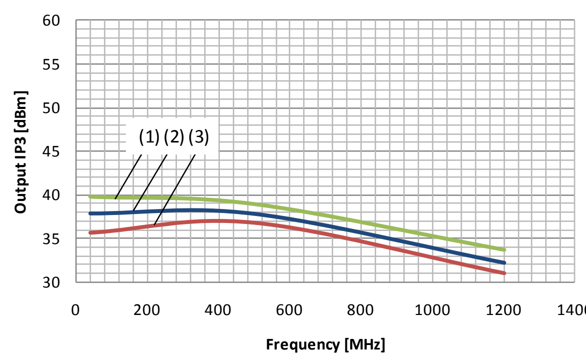
(2) Tamb = +25 °C

(3) Tamb = +85 °C

Fig 28. Output IP3; Vcc = 8 V, IDC CTRL = 3.3 V or open



a. f2 = f1 ± 1 MHz , output power = 10 dBm per frequency.



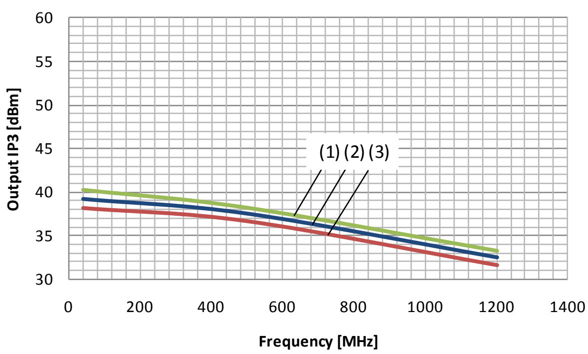
b. f2 = f1 ± 6 MHz , output power = 10 dBm per frequency.

(1) Tamb = -40 °C

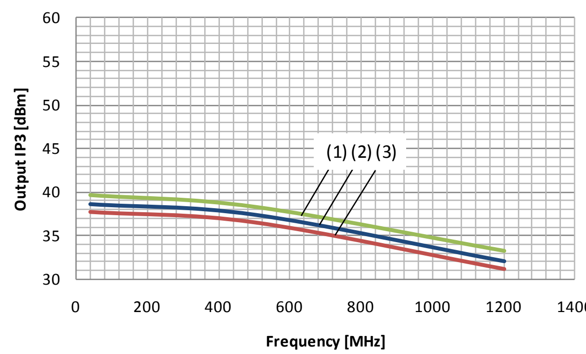
(2) Tamb = +25 °C

(3) Tamb = +85 °C

Fig 29. Output IP3; Vcc = 8 V, IDC CTRL = 0



a. f2 = f1 ± 1 MHz , output power = 10 dBm per frequency.



b. f2 = f1 ± 6 MHz , output power = 10 dBm per frequency.

(1) Tamb = -40 °C

(2) Tamb = +25 °C

(3) Tamb = +85 °C

Fig 30. Output IP3; Vcc = 5 V, IDC CTRL = 0 V

6. Abbreviations

Table 2. Abbreviations

Acronym	Description
AC	Alternating Current
CATV	Community Antenna TeleVision
DC	Direct Current
ESD	Electro Static Discharge
MMIC	Monolithic Microwave Integrated Circuit
NTSC	National Television Standards Committee
PCB	Printed Circuit Board
RF	Radio Frequency
SMD	Surface Mounted Device

7. Legal information

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